

CLAIMS

1. A microcomputer having an on-chip debugging function, comprising:

5 a central processing unit for executing instructions; and  
a first monitor means for performing data transfer to and from a second monitor means, determining a primitive command to be executed based on the receive data from said second monitor means, and performing processing for execution of the determined primitive  
10 command, said second monitor means being provided outside said microcomputer for performing a processing to convert a debugging command into at least one primitive command.

2. The microcomputer according to claim 1, wherein said  
15 primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

20 3. The microcomputer according to claim 1, further comprising a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

25 4. The microcomputer according to claim 2, further comprising a control register used for execution of instructions in said central processing unit and having an address thereof allocated

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on the memory map in the debugging mode.

5. The microcomputer according to claim 1, further comprising a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

6. The microcomputer according to claim 2, further comprising a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on the memory map in the debugging mode.

7. The microcomputer according to claim 1, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor means,

wherein, on condition that said first monitor means being a slave has received data from said second monitor means being a master, said first monitor means performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor means.

8. The microcomputer according to claim 2, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor means,

wherein, on condition that said first monitor means being

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a slave has received data from said second monitor means being a master, said first monitor means performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor means.

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9. The microcomputer according to claim 1, wherein the data received from said second monitor means includes an identification data of the primitive command to be executed by said first monitor means.

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10. The microcomputer according to claim 2, wherein the data received from said second monitor means includes an identification data of the primitive command to be executed by said first monitor means.

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11. The microcomputer according to claim 1, wherein said first monitor means transfers fixed-length data to and from said second monitor means.

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12. The microcomputer according to claim 2, wherein said first monitor means transfers fixed-length data to and from said second monitor means.

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13. The microcomputer according to claim 1, wherein a monitor program for executing a processing of said first monitor means is stored in a ROM.

14. The microcomputer according to claim 2, wherein a monitor program for executing a processing of said first monitor means is stored in a ROM.

15. The microcomputer according to claim 1,  
wherein said first monitor means comprises:  
a first frequency division circuit for dividing a first clock  
and for generating a first sampling clock for sampling each bit  
in data sent and received according to start-stop synchronization;

and

a circuit for sending and receiving data based on said first  
sampling clock, and

wherein said first monitor means supplies said first clock  
to said second monitor means as a signal for causing a second  
frequency division circuit included in said second monitor means  
to generate a second sampling clock.

16. The microcomputer according to claim 2,  
wherein said first monitor means comprises:  
a first frequency division circuit for dividing a first clock  
and for generating a first sampling clock for sampling each bit  
in data sent and received according to start-stop synchronization;  
and

a circuit for sending and receiving data based on said first  
sampling clock, and

wherein said first monitor means supplies said first clock  
to said second monitor means as a signal for causing a second

frequency division circuit included in said second monitor means  
to generate a second sampling clock.

17. The microcomputer according to claim 1 wherein:

5 said first monitor means includes a monitor RAM which is  
readable and writable, and

when a break of an execution of an user program occurs and  
a mode is shifted to a debugging mode, said first monitor means  
saves a program counter value of said central processing unit and  
10 contents of an internal register into said monitor RAM.

18. The microcomputer according to claim 2 wherein:

said first monitor means includes a monitor RAM which is  
readable and writable, and

15 when a break of an execution of an user program occurs and  
a mode is shifted to a debugging mode, said first monitor means  
saves a program counter value of said central processing unit and  
contents of an internal register into said monitor RAM.

20 19. An electronic instrument comprising:

a microcomputer according to claim 1;

an input source of data to be processed by said microcomputer;

and

an output device for outputting data processed by said  
25 microcomputer.

20. An electronic instrument comprising:

a microcomputer according to claim 2;  
an input source of data to be processed by said microcomputer;

and

an output device for outputting data processed by said  
5 microcomputer.

21. An electronic instrument comprising:  
a microcomputer according to claim 3;  
an input source of data to be processed by said microcomputer;

10 and

an output device for outputting data processed by said  
microcomputer.

22. An electronic instrument comprising:  
15 a microcomputer according to claim 5;  
an input source of data to be processed by said microcomputer;

and

an output device for outputting data processed by said  
microcomputer.

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23. An electronic instrument comprising:  
a microcomputer according to claim 7;  
an input source of data to be processed by said microcomputer;

and

25 an output device for outputting data processed by said  
microcomputer.

24. An electronic instrument comprising:  
a microcomputer according to claim 9;  
an input source of data to be processed by said microcomputer;  
and  
5 an output device for outputting data processed by said  
microcomputer.

25. An electronic instrument comprising:  
a microcomputer according to claim 11;  
10 an input source of data to be processed by said microcomputer;  
and  
an output device for outputting data processed by said  
microcomputer.

26. An electronic instrument comprising:  
a microcomputer according to claim 13;  
15 an input source of data to be processed by said microcomputer;  
and  
an output device for outputting data processed by said  
20 microcomputer.

27. An electronic instrument comprising:  
a microcomputer according to claim 15;  
an input source of data to be processed by said microcomputer;  
25 and  
an output device for outputting data processed by said  
microcomputer.

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28. An electronic instrument comprising:  
 a microcomputer according to claim 17;  
 an input source of data to be processed by said microcomputer;  
 5 and  
 an output device for outputting data processed by said  
 microcomputer.

29. A debugging system for a target system including a  
 10 microcomputer, said debugging system comprising:  
 second monitor means for performing processing for  
 converting a debugging command issued by a host system into at least  
 one primitive command; and  
 first monitor means for performing data transfer to and from  
 15 said second monitor means, determining a primitive command to be  
 executed based on the receive data from said second monitor means,  
 and performing processing for execution of the determined primitive  
 command.

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